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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,532	12/27/2001	Ryouichirou Nagamine	PNDF-01197	9433

21254 7590 05/18/2005

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,532	NAGAMINE ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 0701* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-14 are presented for examination.

Response to Arguments

Applicant's arguments filed November 24, 2004 have been fully considered but they are not persuasive.

Applicant argues that the present application presents claims which applicant states "The scan path of the test circuit of the claimed invention differs in an unobvious manner from that of Whetsel and the acknowledged prior art." Applicant also states "The claimed scan paths permit faster testing as set forth in the specification, for example at page 18, line 24 to page 19, line 7." The examiner would like to point out that regardless of how well the specification describes the invention, the claims must clearly define the claimed portion of the disclosure. The claims set forth in the present application do not clearly differentiate over the cited prior art as described below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, line 2 recites 'a first output terminal' without further reference to a second or third etc. output terminal, otherwise it is unclear the need for designating an output terminal as 'a first output terminal'. If the applicant is intending this wording to distinguish the functional output terminal over the scan output terminal, the claims should be worded as such.

Line 3 recites 'a plurality of flip-flops', and line 7 recites 'a like plurality of logic gates', which would indicate to the examiner that there are the same number of each (logic gates and flip flops). Lines 7-9 state "each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip flops'. This statement leads the examiner to associate a one to one correspondence between each flip-flop and 'respective' logic gate. However, in lines 11-12, applicant states 'serially connecting at least some of said plurality of flip-flops through the respective logic gates'. This statement seems to negate the above correspondence or one to one association as indicated in lines 7-9.

Line 14 again indicates the presence of other output terminals that are not mentioned in the claim by stating 'the first output'.

Also, as stated in the previous office action, the claimed 'logic gates' (line 7) stating 'a like plurality of logic gates, each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip flops', these 'logic gates' are claimed vaguely and not as required (particularly point out and distinctly claiming) as required by the second paragraph of 35 U.S.C. 112.

As per claim 2, line 2 recites 'a first input terminal' without further reference to a second or third etc. output terminal, otherwise it is unclear the need for designating an output terminal as 'a first output terminal'. If the applicant is intending this wording to distinguish the functional output terminal over the scan output terminal, the claims should be worded as such.

Line 3 recites 'a plurality of flip-flops', and line 6 recites 'a like plurality of logic gates', which would indicate to the examiner that there are the same number of each (logic gates and flip flops). Lines 6-8 state "each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip flops'. This statement leads the examiner to associate a one to one correspondence between each flip-flop and 'respective' logic gate. However, in lines 10-11, applicant states 'serially connecting at least some of said plurality of flip-flops through the respective logic gates'. This statement seems to negate the above correspondence or one to one association as indicated in lines 6-8.

Line 13 again indicates the presence of other input terminals that are not mentioned in the claim by stating 'the first input'.

Also, as stated in the previous office action, the claimed 'logic gates' (line 6) stating 'a like plurality of logic gates, each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip flops', these 'logic gates' are claimed vaguely and not as required (particularly point out and distinctly claiming) as required by the second paragraph of 35 U.S.C. 112.

Claims 3-7 have the same issues as brought up in the previous rejection of claims 1 and 2. Claims 8-14 also have many of the same second paragraph of 35 U.S.C. 112 issues with the exception of the logic gate issues. Each of these claims recites a first (input and/or output) terminal with no following reference to any additional input and/or output terminal.

Therefore based upon the ambiguity of the presented claims, the examiner will maintain the previous rejection as stated in the prior office action based upon the examiner's understanding of the presented claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Whetsel U. S. Patent No. 6,199,182.

As per claims 1-3, Whetsel teaches that scan testing of circuits is well known. Scan testing configures the circuit into scan cells and combinational logic. Once so

configured, the scan cells are controlled to capture test response data from the combinational logic, then shifted to unload the captured test response data from the combinational logic and to load the next test stimulus data to apply to the combinational logic. Also, in FIG. 39A, the tester includes a conventional scan interface for controlling scan operations, signal generators for producing DC and AC test signals, voltmeters for measuring DC and AC voltages, a first switching circuit (SW1) for connecting the tester's TSA or TSB terminals to the voltmeter or signal generators, a second switch circuit (SW2) for connecting the tester's TSC terminal, through a known resistor R, to a programmable voltage source (Vp), and a conventional test control computer for controlling the overall operation of the tester. (Figure 39A, column 1 lines 18-24, column 20 lines 4-13)

As per claims 4-7, Whetsel teaches that scan testing of circuits is well known. Scan testing configures the circuit into scan cells and combinational logic. Once so configured, the scan cells are controlled to capture test response data from the combinational logic, then shifted to unload the captured test response data from the combinational logic and to load the next test stimulus data to apply to the combinational logic. Also, in FIG. 39A, the tester includes a conventional scan interface for controlling scan operations, signal generators for producing DC and AC test signals, voltmeters for measuring DC and AC voltages, a first switching circuit (SW1) for connecting the tester's TSA or TSB terminals to the voltmeter or signal generators, a second switch circuit (SW2) for connecting the tester's TSC terminal, through a known resistor R, to a

programmable voltage source (Vp), and a conventional test control computer for controlling the overall operation of the tester. FIG. 1 shows an electrical circuit having three memories (M) A, B, C and combinational logic (CL). FIG. 2 shows an example of the memories of FIG. 1 implemented as D flip-flops (FF), each memory having a data input, data output, and clock and reset control signals. FIG. 3 shows one example of how the circuit of FIG. 1 can be made scan testable by converting the memories into scan cells and connecting the outputs (D, E, F) of the combinational logic to the scan cell capture inputs. FIG. 4A shows an example of how a D flip flop based memory is converted into a scan cell. The scan cells have a 3:1 multiplexer input to the flip-flop. The multiplexer receives selection control (S) to: (1) input the output of the combinational logic to the flip flop (Input1, the capture input), (2) input the external input to the flip flop (Input2, the functional input), or (3) input the serial input to the flip-flop (SI, the shift input). The flip-flop receives a clock (C) and a reset (R) control input. The scan cells are connected together via their serial input (SI) and serial output (SO) to form a 3-bit scan path through the circuit of FIG. 3. The three scan cells operate as the state memories during functional operation. During test operation, the scan cells operate as scan cells to allow inputting test stimulus to the combinational logic and capturing the response output from the combinational logic. While edge sensitive D flip-flop memories are used in this disclosure, level sensitive memories could be used as well. (Figures 1-4 and 39A, column 1 lines 18-50, column 20 lines 4-13)

As per claims 8-10, Whetsel teaches that scan testing of circuits is well known. Scan testing configures the circuit into scan cells and combinational logic. Once so configured, the scan cells are controlled to capture test response data from the combinational logic, then shifted to unload the captured test response data from the combinational logic and to load the next test stimulus data to apply to the combinational logic. Also, in FIG. 39A, the tester includes a conventional scan interface for controlling scan operations, signal generators for producing DC and AC test signals, voltmeters for measuring DC and AC voltages, a first switching circuit (SW1) for connecting the tester's TSA or TSB terminals to the voltmeter or signal generators, a second switch circuit (SW2) for connecting the tester's TSC terminal, through a known resistor R, to a programmable voltage source (Vp), and a conventional test control computer for controlling the overall operation of the tester. (Figure 39A, column 1 lines 18-24, column 20 lines 4-13)

As per claims 11-14, Whetsel teaches that scan testing of circuits is well known. Scan testing configures the circuit into scan cells and combinational logic. Once so configured, the scan cells are controlled to capture test response data from the combinational logic, then shifted to unload the captured test response data from the combinational logic and to load the next test stimulus data to apply to the combinational logic. Also, in FIG. 39A, the tester includes a conventional scan interface for controlling scan operations, signal generators for producing DC and AC test signals, voltmeters for measuring DC and AC voltages, a first switching circuit (SW1) for connecting the tester's TSA or TSB terminals to the voltmeter or signal generators, a second switch

circuit (SW2) for connecting the tester's TSC terminal, through a known resistor R, to a programmable voltage source (Vp), and a conventional test control computer for controlling the overall operation of the tester. FIG. 1 shows an electrical circuit having three memories (M) A, B, C and combinational logic (CL). FIG. 2 shows an example of the memories of FIG. 1 implemented as D flip-flops (FF), each memory having a data input, data output, and clock and reset control signals. FIG. 3 shows one example of how the circuit of FIG. 1 can be made scan testable by converting the memories into scan cells and connecting the outputs (D, E, F) of the combinational logic to the scan cell capture inputs. FIG. 4A shows an example of how a D flip flop based memory is converted into a scan cell. The scan cells have a 3:1 multiplexer input to the flip-flop. The multiplexer receives selection control (S) to: (1) input the output of the combinational logic to the flip flop (Input1, the capture input), (2) input the external input to the flip flop (Input2, the functional input), or (3) input the serial input to the flip-flop (SI, the shift input). The flip-flop receives a clock (C) and a reset (R) control input. The scan cells are connected together via their serial input (SI) and serial output (SO) to form a 3-bit scan path through the circuit of FIG. 3. The three scan cells operate as the state memories during functional operation. During test operation, the scan cells operate as scan cells to allow inputting test stimulus to the combinational logic and capturing the response output from the combinational logic. While edge sensitive D flip-flop memories are used in this disclosure, level sensitive memories could be used as well. (Figures 1-4 and 39A, column 1 lines 18-50, column 20 lines 4-13)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
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